

FIG. 1 is a block diagram of a clock phase determination circuit. The circuit includes a Multiphase Clock Generating Circuit (10) which receives an input signal DIN and an output signal OUTCLK. The Multiphase Clock Generating Circuit (10) generates multiple clock signals, including CLK1, CLK2, and CLKn. A Latch Control Circuit (40) receives the input signal DIN and outputs a latch control signal LC. A series of flip-flops (FF1, FF2, ..., FFn) are connected in a chain. The clock inputs of FF1 and FF2 are connected to CLK1 and CLK2, respectively. The output of FF1 is connected to the input of FF2. The output of FF2 is connected to the input of the Latch Circuit (30). The Latch Circuit (30) is clocked by the LC signal and outputs a signal to the Clock Phase Determination Circuit (50). The Clock Phase Determination Circuit (50) outputs the signal CSL. A Selector (60) receives the CLKn signal and outputs the OUTCLK signal.

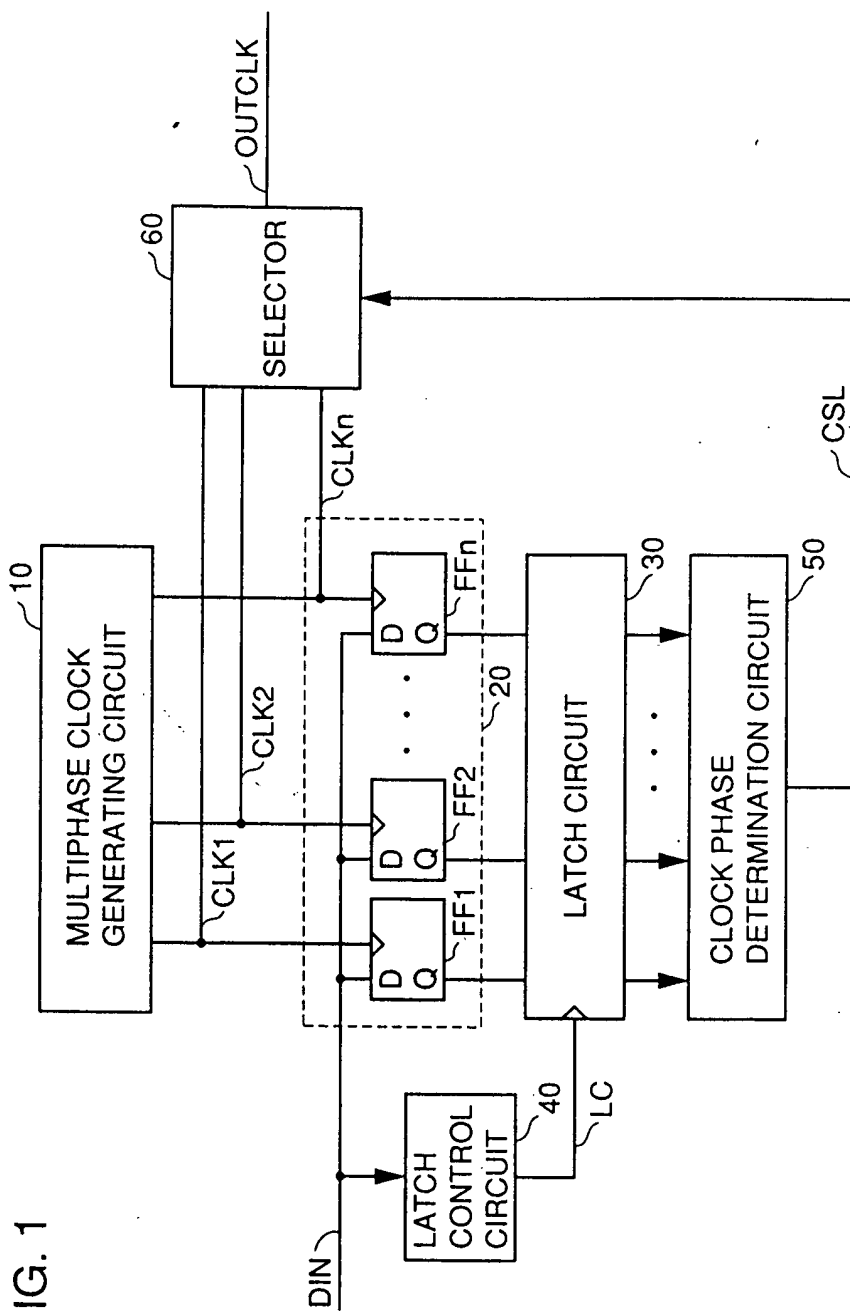
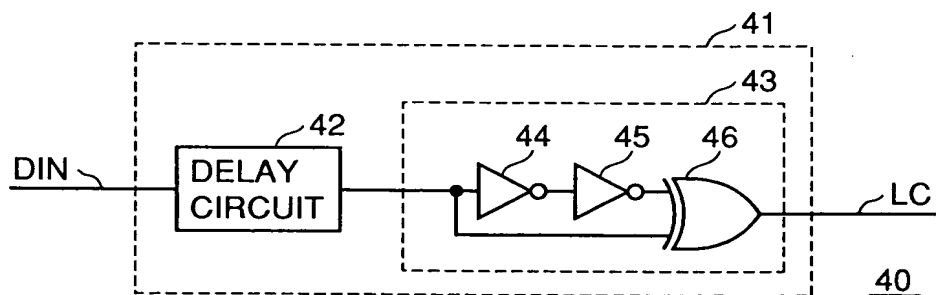
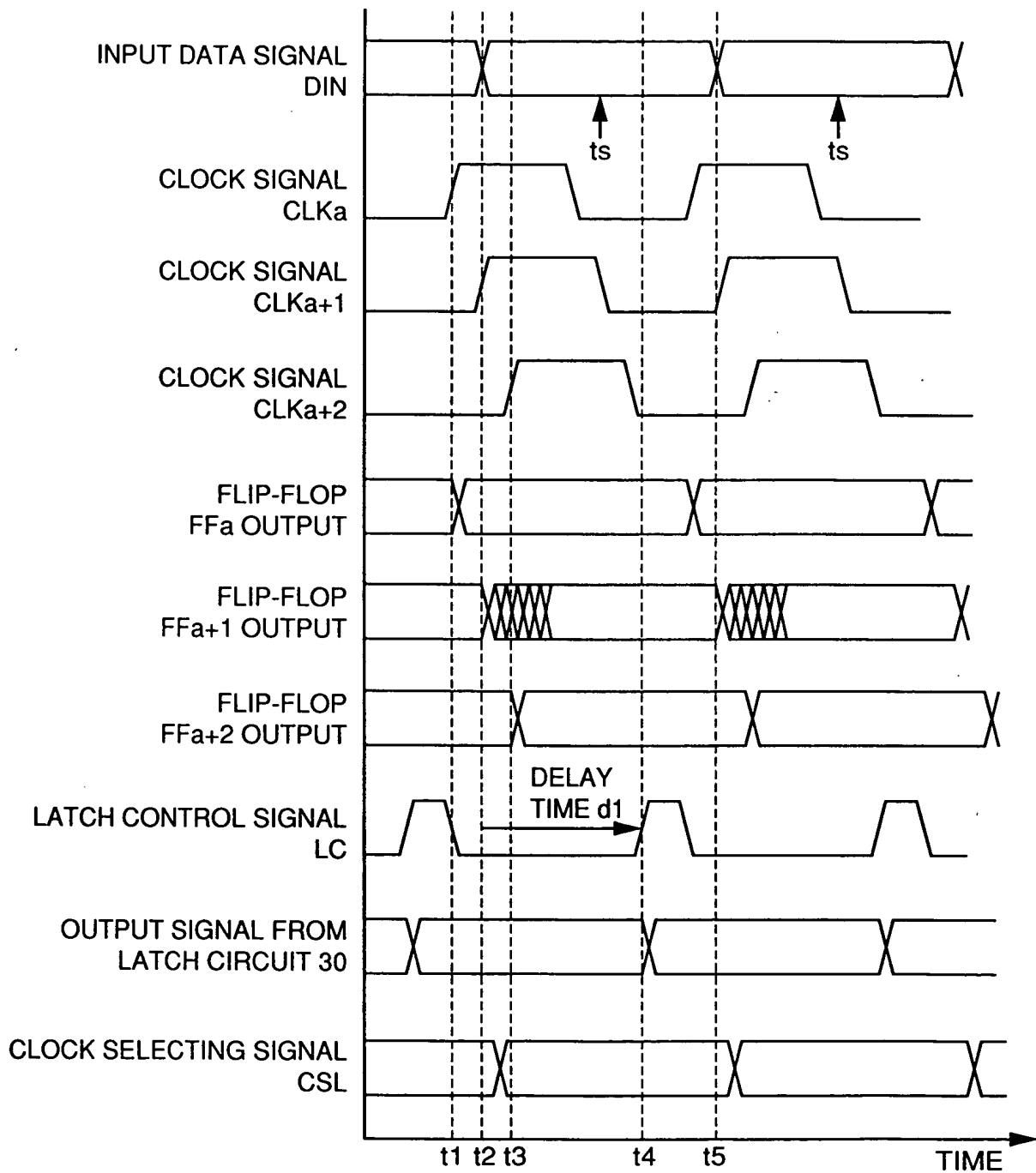


FIG. 2



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FIG. 3



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FIG. 4

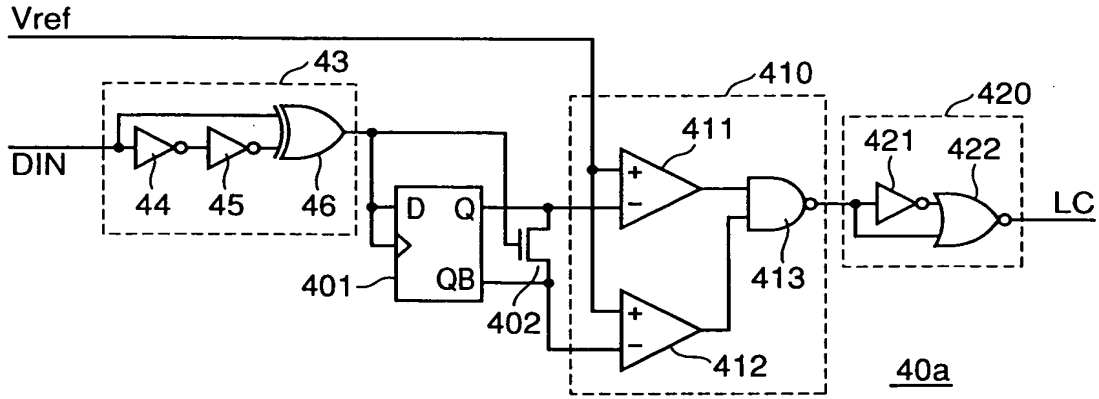
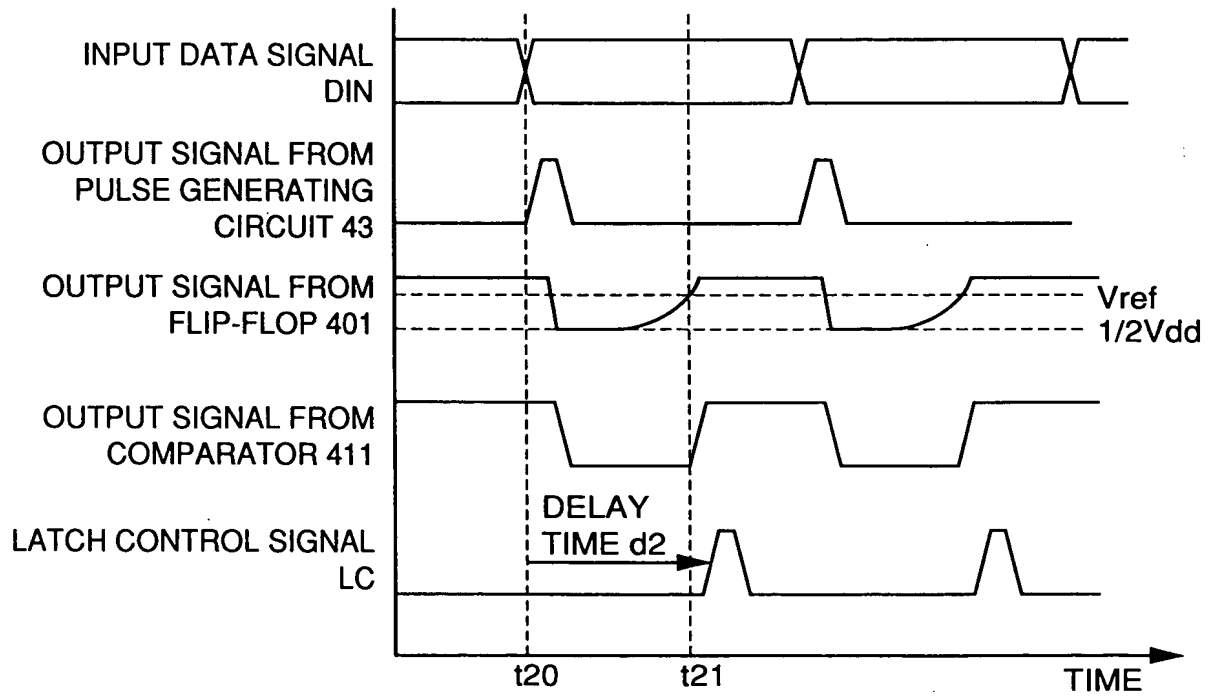


FIG. 5



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FIG. 6

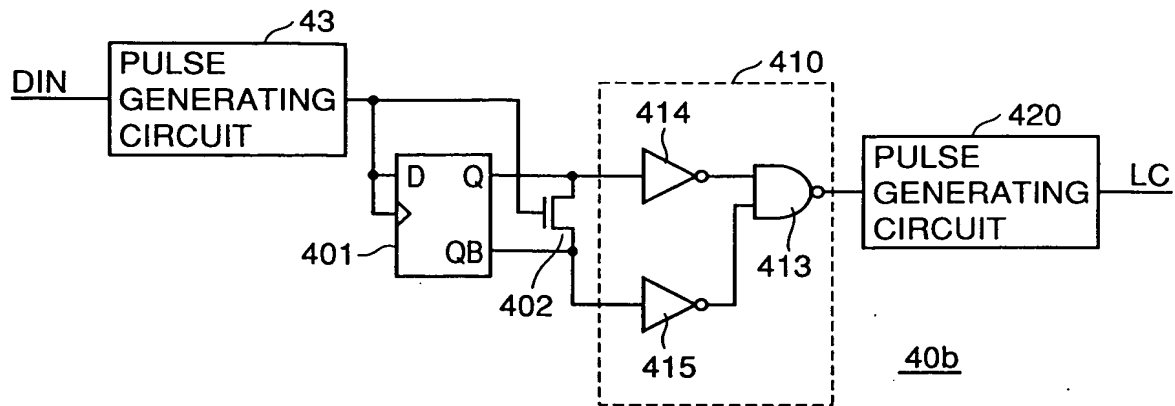
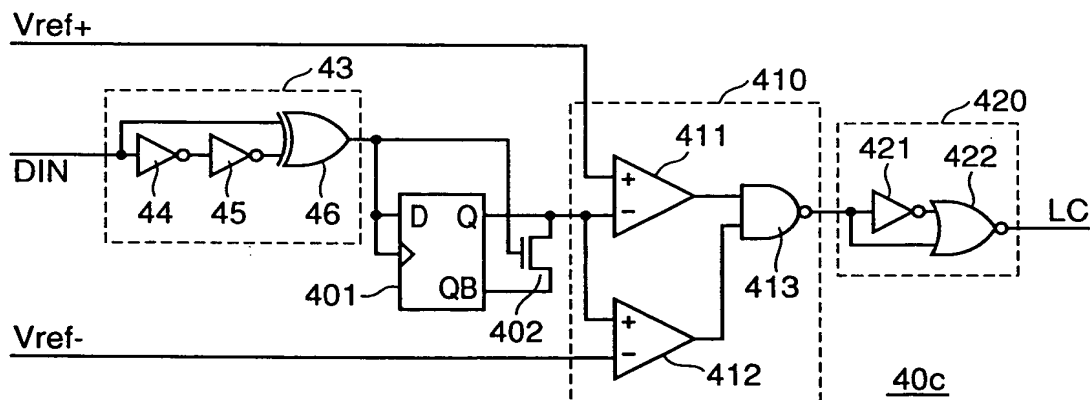
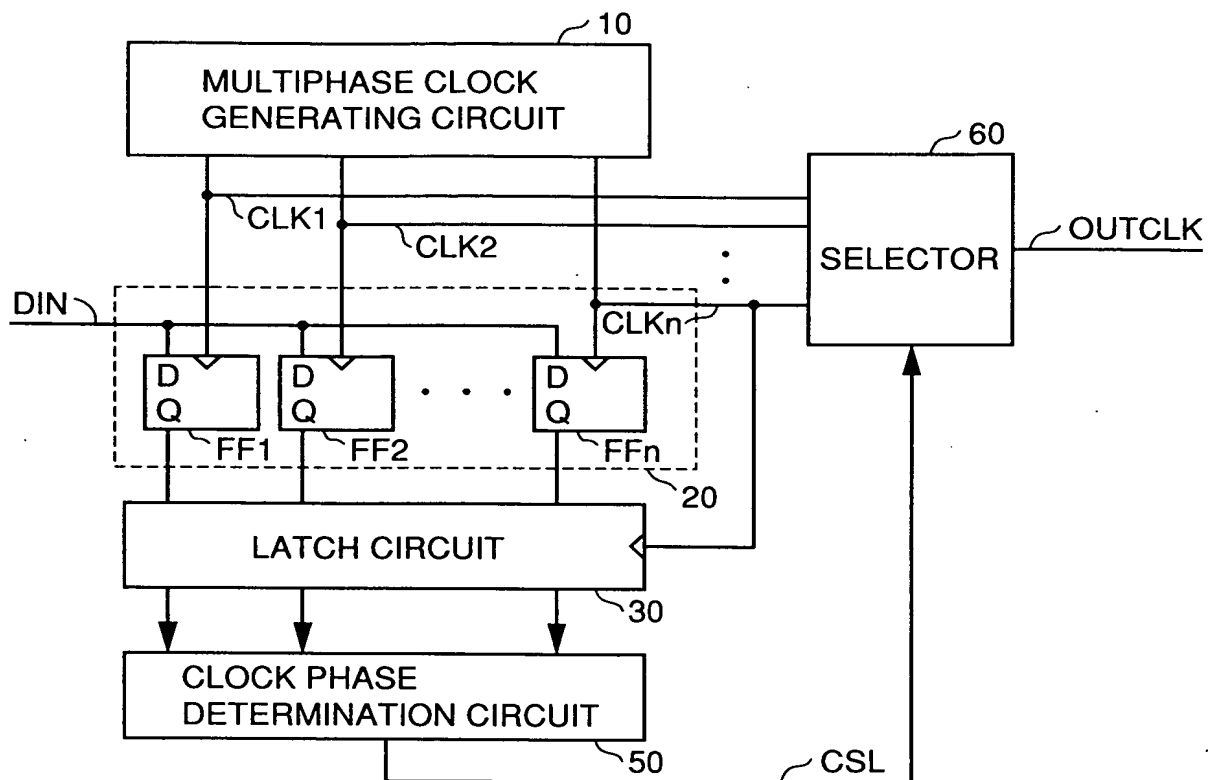


FIG. 7



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FIG. 8 PRIOR ART



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